pattern as recited in claim 2. Therefore, Ikegami does not disclose each and every element of the process recited in claim 2, and Ikegami does not disclose each and every such element arranged as recited in claim 2. Consequently, claim 2 does not read on Ikegami and thus Ikegami may not anticipate claim 2.

Claim 1 in its present form recites, *inter alia*, selectively removing at a total etch pressure in the range from about 1 millitorr to about 400 millitorr. In contrast Ikegami discloses selective etching only at the "high pressure of 1.0 Torr." Ikegami, p. 1556, left col., p. 1557, left col. Therefore, Ikegami does not disclose each and every element of the process recited in claim 1, and Ikegami does not disclose each and every such element arranged as recited in claim 1. Consequently, claim 1 does not read on Ikegami and thus Ikegami may not anticipate claim 1.

Applicant respectfully submits that claims 1-2 patentably distinguish over Ikegami, and reconsideration and withdrawal of this rejection is respectfully requested.

**2.2. *Claim Rejections Under 35 U.S.C. § 103(a)***

The claims pending prior to this Amendment "D" and Response stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ikegami as applied in the anticipation rejection addressed in the foregoing subsection. Office Action, pp. 2-5, item 19.

Ikegami investigates mechanisms to understand the differences in the surface condition of individual films of PSG and $SiO_2$ during etching with a mixture of $CF_4/CHF_3/Ar$ at the high pressure of 1.0 Torr and at a low wafer temperature. *See, e.g.*, Ikegami, p. 1556, left col. Ikegami reports that PSG reacts more rapidly than $SiO_2$ under such etching conditions (hereinafter referred to as the "PSG/$SiO_2$ selectivity"). *See, e.g.*, Ikegami, p. 1556, left col. The PSG/$SiO_2$ selectivity reported in Ikegami is attributed to and explained in terms of the presence of phosphorous in PSG, and more particularly to the existence of phosphorous-oxygen bonds (P-O and P=O bonds) and to the existence of phosphoric oxide in PSG. *See, e.g.*, Ikegami, p. 1560, § 4, p. 1561, § 5.

As set forth in the Office Action, Ikegami neither discloses nor suggests any of the following elements and features in the claims:

(1) formation of a via in a doped $SiO_2$ layer by its selective etching with an undoped $SiO_2$ etch stop;

(2) formation of a via as indicated at (1) by further using a patterned photo resist etch mask;

(3) formation of a SAC through a PSG ILD layer which covers gates on a wafer where the gates are capped with undoped $SiO_2$;

(4) the formation referred to at (3) further incorporating gate sidewall spacers;

(5) formation of gates on a wafer with refractory metal silicide; and

(6) the etch parameters recited in the claims, which include plasma density, etch pressure, plasma etch reactor cathode temperature, semiconductor material temperature, material removal rate upon etching, chemical composition of the etchant; etching techniques, and chemical composition of the different structural elements of the semiconductor structure.

In addition to the foregoing elements and features, Ikegami does not disclose or suggest various additional elements and features such as the following:

(7) the use of undoped $SiO_2$ as an effective etch stop to solve the problems and avoid the adverse consequences that derive from the conventional use of silicon nitride caps in alignment processes and as etch stops;

(8) the use of undoped $SiO_2$ as indicated at (8) will not be accompanied by the problems and detrimental consequences that afflict the conventional techniques that rely on silicon nitride caps;

(9) differences in etch selectivity regarding undoped $SiO_2$ on the one hand, and doped $SiO_2$ on the other hand, will effectively lead to the formation of self-aligned contacts;

(10) the amount of etch selectivity that will accomplish the results indicated at (9);

(11) the existence of any etch selectivity when the doped $SiO_2$ does not contain phosphorous;

(12) the existence of any etch selectivity when the doped $SiO_2$ is different from PSG;

(13) the existence of any etch selectivity when etching is performed at pressures significantly lower than the single pressure of 1.0 Torr;

(14) the implementation and use of PSG/$SiO_2$ selectivity under conditions other than the limited and narrow conditions indicated above and with structures and processes that go beyond the structureless isolated PSG and $SiO_2$ layers used by Ikegami;

(15) the implementation and use of doped $SiO_2$ (other than PSG)/$SiO_2$ selectivity under any conditions at all, including the limited and narrow conditions indicated above and the structureless isolated layers used by Ikegami; and

(16) the effective and successful implementation of the features indicated above in the context of increasing miniaturization in the process of forming contact openings and contacts in semiconductor devices, in the process of forming gate structures, and in the process of forming self-aligned contacts in semiconductor devices.

For at least the reasons set forth above, Ikegami discloses a process that is different from the claimed processes. These differences include differences in kind of process steps, materials, conditions, and structures. Ikegami discloses a process that relies on conditions, including structures and compositions, that are different from those used in the claimed processes. Ikegami discloses a process that does not teach or suggest its use in effectively achieving the formation of precisely aligned structural features in complex miniature devices as it is accomplished by the claimed processes. Ikegami discloses a process that does not teach or suggest how to modify its use to efectively achieve the formation of precisely aligned structural features in complex miniature devices as it is accomplished by the claimed proceses. Ikegami discloses a process that does not teach or suggest the overcoming of prior art problems that the claimed processes

overcome. Differences between the process disclosed in Ikegami and the claimed processes render the claimed processes different in kind and nature from the process disclosed in Ikegami.

Because of differences and limitations such as those described hereinabove, Ikegami has not taught or suggested the claimed processes, and it may not be asserted that the teachings provided by Ikegami are sufficient for one of ordinary skill in the art to make the substitutions, combinations or other modifications that are necessary to arrive to the claimed processes as recited in the pending claims.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-97 (Rev. 1, Feb. 2000). For at least the reasons set forth above, Applicant respectfully submits that these criteria are not satisfied by Ikegami.

Applicant notes the various individual items with respect to which the Office Action takes official notice. However, even if each of such items were individually known, the combination of method steps as presently claimed with the parameters and conditions recited therein are neither taught nor suggested by such items and by Ikegami, whether such items and Ikegami are taken alone or in combination. The items with respect to which official notice is taken and Ikegami do not provide any motivation or suggestion to arrive at the claimed processes and they do not provide any indication that the claimed methods would have any reasonable expectation of success.

Applicant respectfully points out that the prior art has conventionally relied on silicon

nitride caps in alignment processes and that despite the problems and adverse consequences derived from this conventional processes, the conventional techniques have not used methods such as those presently claimed. This long-felt need, accompanied with the patent unavailability among the conventional methods, of processes that solve the problems derived from the use of silicon nitride caps in alignment processes further indicates that the presently claimed methods are not obvious in light of the ordinary skill in the art. To this respect, Applicant points to relevant parts of the Application that are discussed as follows by way of illustration and not to provide any interpretive limitation.

The written description of the present Application (hereinafter the "written description") sets forth a problem associated with greater miniaturization levels of semiconductor devices. This problem derives from the need for exact alignment of a contact hole with an active region in the interconnect structure of an integrated circuit in contact hole patterning and etching operations. *See, e.g.*, Application, p. 3, *ll.* 12-15. Various detrimental consequences derive from the failure to achieve such an exact alignment, as set forth in the written description. *See, e.g.*, Application, p. 3, *ll.* 15-19. Conventional attempts to remedy this problem rely on a silicon nitride layer or cap, conventionally located on top of a gate stack as an etch stop layer during self-aligned contact etch processes. *See, e.g.*, Application, p. 3, *ll.* 21-23.

However, these conventional remedies lead to other problems and adverse consequences of their implementation. As indicated in the written description, for example, forming a silicon nitride cap leads to the simultaneous formation of a silicon nitride layer on the back side of the semiconductor wafer. *See, e.g.*, Application, p. 3, *ll.* 23-25. Additional problems and adverse consequences derived from the conventional formation of a silicon nitride cap arise. These additional problems and adverse consequences include, as set forth in the written description: silicon nitride deposition on both sides of the semiconductor wafer at low pressure CVD; semiconductor wafer deformation due to the presence of silicon nitride on the back of the

semiconductor wafer; potential crystal structure deformation and circuit defects caused by such silicon nitride presence; low yield derived from the abundant particulate matter generation in the silicon nitride deposition; and need to remove the silicon nitride layering on the back side of the semiconductor wafer after a low pressure CVD process. *See, e.g.*, Application, p. 3, *ll.* 25-26, p. 4, *ll.* 1-8. Therefore, numerous adverse consequences derive from the conventional practice with a silicon nitride etch stop layer or cap, and these adverse consequences lead to undesirable characteristics such as defective devices, longer processes, and low yield operations.

The presently claimed processes utilize an etch on doped silicon dioxide with undoped silicon dioxide as an etch stop in the recited semiconductive device manufacturing processes. By overcoming such problems and avoiding their derived adverse consequences, the claimed processes provide results that are different in kind and nature, and not merely in degree, from the results of conventional methods. No prior art of record teaches or suggests such use as recited in the claimed processes for solving problems that afflict the conventional methods as indicated above by the illustrative references to the written description.

Applicant notes the quote and cite to *In re Aller*, 220 F.2d 454 (C.C.P.A. 1955) provided in the Office Action. Applicant respectfully points out that this authority does not apply to the presently recited claims for at least the following reasons.

*In re Aller* establishes as a requisite for its applicability that the general conditions of a claim be disclosed in the prior art. *See, In re Aller*, 220 F.2d at 456. Applicant submits that this requisite is not satisfied in light of the present claims because, as indicated hereinabove, such conditions are not disclosed in the prior art.

The facts as set forth *In re Aller* show that the art of record and the rejected claims in *In re Aller* both used the same reactants to produce the same results or products, but the rejected claims recited different acid concentration and temperature. It was not found in *In re Aller* that changes in such variables introduced differences in kind with respect to the results of the prior

art. *See, In re Aller*, 220 F.2d at 456. Applicant submits that these conditions are not satisfied in light of the present claims because, as indicated hereinabove, the results obtained by the presently claimed processes are different in kind and not merely in degree from those provided by the conventional methodology.

Applicant further submits that the use of the various recited parameters is not the result of mere optimization on the basis of known laws or patterns of behavior, but another manifestation of inventive work that is not taught or suggested by the prior art. For example, Ikegami discloses an etch process that is performed at a single high pressure. Ikegami does not teach or suggest that the claimed processes, that are applied to different structures and/or compositions, would be successful for solving the prior art problems at significantly different pressures. Ikegami teaches that the PSG/$SiO_2$ selectivity reported therein is due to the presence of specific phosphorous-containing bonds in PSG. Ikegami does not teach or suggest what selectivity, including type and extent of any selectivity, would be expected in other forms of phosphorous-doped silicon dioxide, and in silicon dioxide that is doped with elements that are not phosphorous. This lack of teachings and the additional lack of teachings as indicated hereinabove with respect to Ikegami and the officially noticed items distinguish the conditions as set forth in *In re Aller* from those of the presently claimed processes.

Consequently, Applicant respectfully submits that Ikegami does not support a *prima facie* case of obviousness regarding the present claims. Applicant respectfully requests the reconsideration and withdrawal of this rejection.

## 3. CONCLUSIONS

In view of the above, Applicant respectfully maintains that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 19th day of September 2001.

Respectfully submitted,

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**Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):**

Please amend the claims as follows and in accordance with 37 C.F.R. § 1.121(c)(1)(ii), by which Applicant submits the following marked up version only for the claim being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

1. (Twice Amended) A process for forming a contact opening to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of semiconductor material;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

selectively removing[,] by etching at a total etch pressure in the range from about 1 millitorr to about 400 millitorr and by using an etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof, a portion of said doped silicon dioxide layer at a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

6. (Once Amended) A process as recited in Claim 4, wherein said plasma etching process is conducted in a pressure range from about 1 millitorr to about [400] 100 millitorr.

13. (Thrice Amended) A process for forming contact to a semiconductor material, said process comprising:

forming an undoped silicon dioxide layer over a layer of monocrystalline silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist;

etching said doped silicon dioxide layer through the pattern of said layer of photoresist at a material removal rate that is higher for doped silicon dioxide layer than for undoped silicon dioxide layer or for said layer of monocrystalline silicon to form an opening extending to said layer of monocrystalline silicon, said etching being a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about $10^9$ ions/cm$^3$ to about $10^{13}$ ions/cm$^3$ with a fluorinated chemical etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof.

30. (Twice Amended) A process as recited in Claim 29, wherein said fluorinated chemical etchants is selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof.

31. (Thrice Amended) A process for forming a contact to a semiconductor material comprising:

depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

depositing a polysilicon layer over said gate oxide layer;

depositing a refractory metal silicide layer over said polysilicon layer;

depositing an undoped silicon dioxide layer over said refractory metal silicide layer;

selectively removing portions of said undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side perpendicular to said gate oxide layer and being comprised of:

said undoped silicon dioxide layer as the top layer thereof;

said refractory metal silicide layer;

said polysilicon layer; and

said gate oxide layer as the bottom layer thereof;

forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

etching said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about $10^9$ ions/cm$^3$ to about $10^{13}$ ions/cm$^3$ in an etcher selected from the group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from

about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof.

37. (Thrice Amended) A process for forming a gate structure comprising:

providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

removing said first layer of photoresist;

depositing a doped silicon dioxide layer over said multilayer structure;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch that is an anisotropic plasma etch using fluorinated chemical etchants selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof, and that etches through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide,

photoresist, or nonconductive material;

removing said second layer of photoresist; and

forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

44. (Thrice Amended) A process for forming a gate structure comprising:

providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

depositing a layer of undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

removing said first layer of photoresist;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG;

forming a second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for undoped silicon dioxide, photoresist, or

nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof, wherein said etching of said doped silicon dioxide utilizes a plasma etching system having a plasma density in a range from about $10^9$ ions/cm$^3$ to about $10^{13}$ ions/cm$^3$ at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

removing said second layer of photoresist; and

forming a contact plug comprising a conductive material in contact with said contact surface on said layer of silicon.

50. (Thrice Amended) A method of forming a self-aligned contact, said method comprising:

providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by an undoped silicon dioxide layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

forming a layer of photoresist over said silicon dioxide layer;

patterning said layer of photoresist; and

selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks using an etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $CH_2F_2$, $C_2HF_5$, [and] $CH_3F$, and combinations thereof, to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing less of said undoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

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